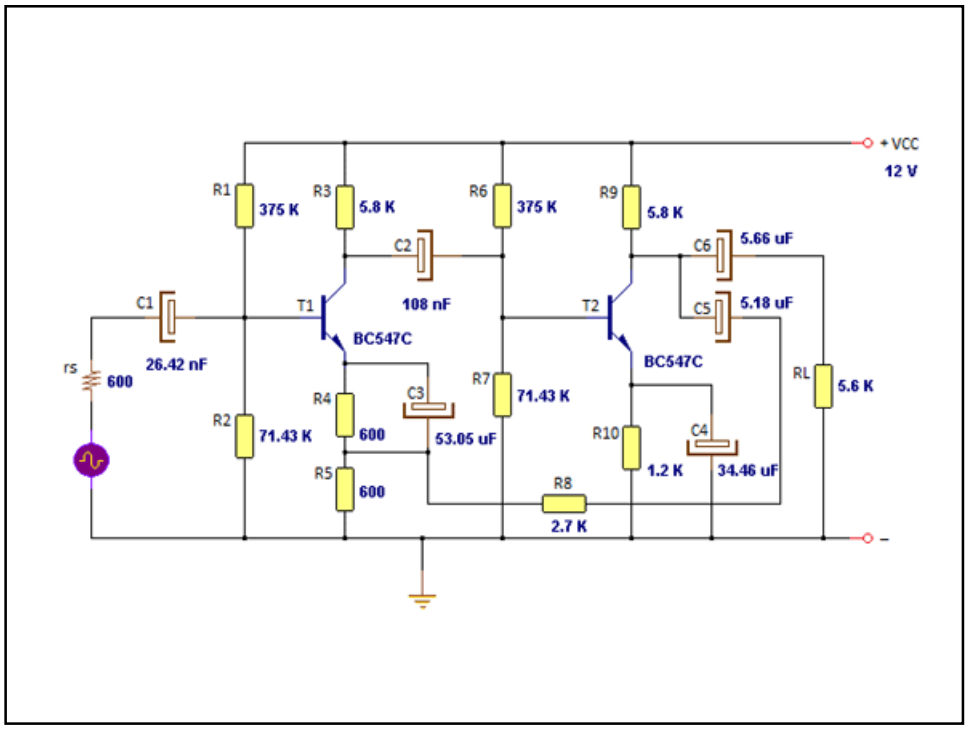
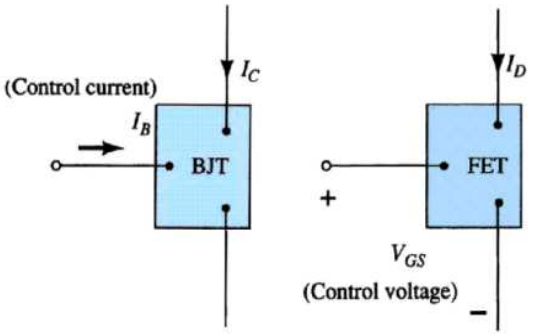


Introduction to FET's

Current Controlled vs Voltage Controlled Devices



3

Types of FET's

- JFET – Junction Field Effect Transistor
- MOSFET – Metal Oxide Semiconductor Field Effect Transistor
  - D-MOSFET - Depletion Mode MOSFET
  - E- MOSFET - Enhancement Mode MOSFET

4

Transfer Characteristics

The input-output transfer characteristic of the JFET is not as straight forward as it is for the BJT

In a BJT, β (h_{FE}) defined the relationship between I_B (input current) and I_C (output current).

In a JFET, the relationship (Shockley's Equation) between V_{GS} (input voltage) and I_D (output current) is used to define the transfer characteristics, and a little more complicated (and not linear):

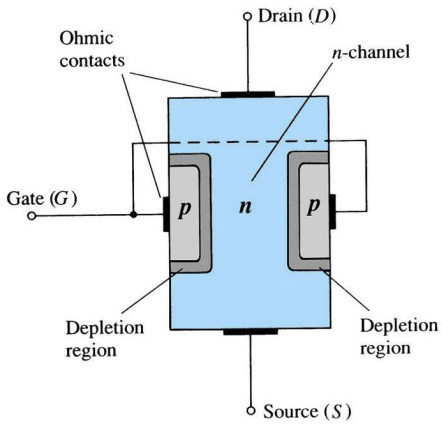
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

As a result, FET's are often referred to a square law devices

5

JFET Construction

There are two types of JFET's: n-channel and p-channel.
The n-channel is more widely used.



There are three terminals: Drain (D) and Source (S) are connected to n-channel
Gate (G) is connected to the p-type material

6

JFET Operating Characteristics

There are three basic operating conditions for a JFET:
JFET's operate in the depletion mode only

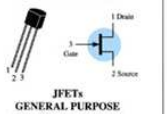
A. $V_{GS} = 0$, V_{DS} is a minimum value depending on I_{DSS} and the drain and source resistance
B. $V_{GS} < 0$, V_{DS} at some positive value and
C. Device is operating as a Voltage-Controlled Resistor

For an n channel JFET, V_{GS} may never be positive*
For an p channel JFET, V_{GS} may never be negative*

7

Specification Shet (JFETs)

2N5457
CASE 29-04, STYLE 5
TO-92 (TO-226AA)



JFETs
GENERAL PURPOSE
N-CHANNEL—DEPLETION

Refer to 2N4220 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	-25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	-25	–	–	Vdc
Gate Reverse Current (V_{GS} = -15 Vdc, V_{DS} = 0) (V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)		I_{GSS}	– –	– –	-1.0 -200	nAdc
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	-0.5	–	-6.0	Vdc
Gate Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc)	2N5457	V_{GS}	–	-2.5	–	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5457	$\|y_{fs}\|$	1000	–	5000	μmhos
Output Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|y_{os}\|$	–	10	50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	3.0	pF

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

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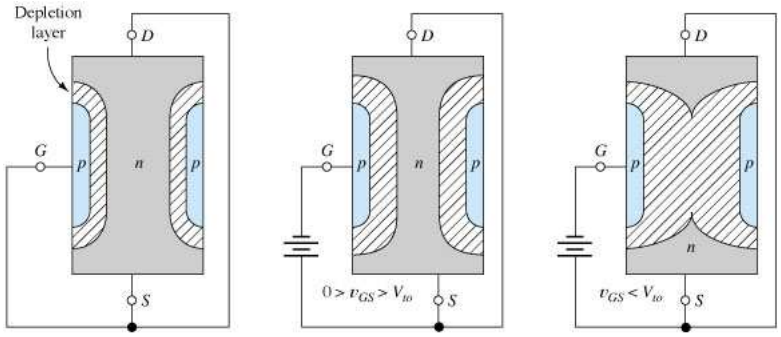
N-Channel JFET Operation



(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source

(b) Moderate gate-to-channel reverse bias results in narrower channel

(c) Bias greater than pinch-off voltage; no conductive path from drain to source

The nonconductive depletion region becomes thicker with increased reverse bias. (*Note:* The two gate regions of each FET are connected to each other.)

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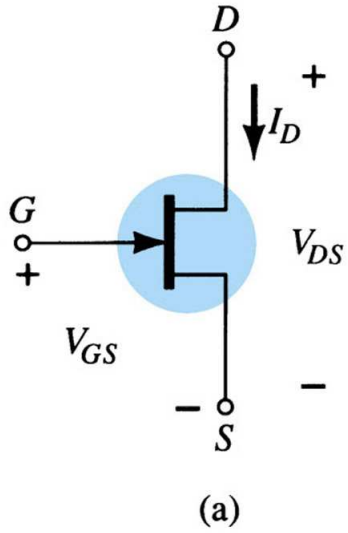
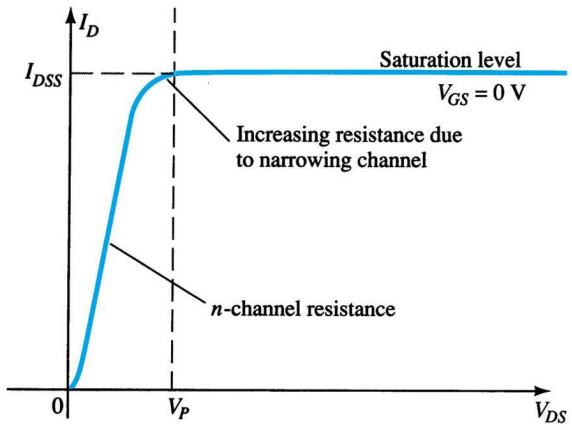
N-Channel JFET Symbol



(a)

10

Saturation



At the pinch-off point:

- any further increase in V_{GS} does not produce any increase in I_D. V_{GS} at pinch-off is denoted as Vp.
- ID is at saturation or maximum. It is referred to as I_{DSS}.
- The ohmic value of the channel is at maximum.

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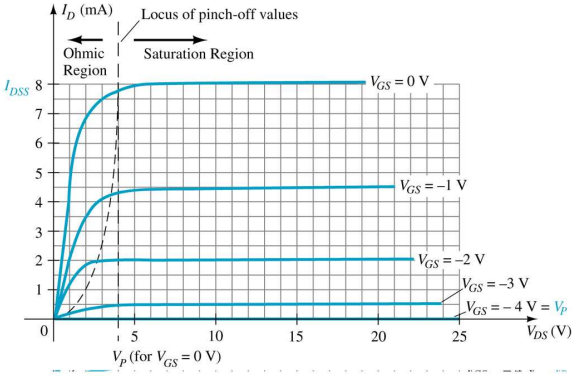
$I_D \leq I_{DSS}$



As V_{GS} becomes more negative:

- the JFET will pinch-off at a lower voltage (Vp).
- I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.
- Eventually I_D will reach 0A. V_{GS} at this point is called Vp or $V_{GS(off)}$.
- Also note that at high levels of V_{DS} the JFET reaches a breakdown situation. ID will increases uncontrollably if $V_{DS} > V_{DSmax}$.

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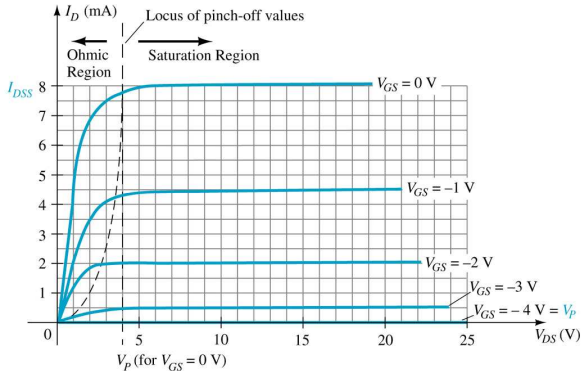
FET as a Voltage-Controlled Resistor



The region to the left of the pinch-off point is called the ***ohmic region***.

The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

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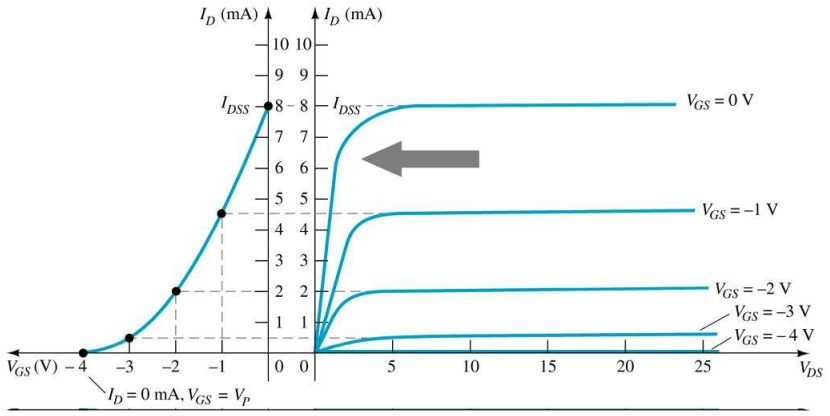
Transfer (Transconductance) Curve



From this graph it is easy to determine the value of I_D for a given value of V_{GS}

It is also possible to determine I_{DSS} and V_P by looking at the knee where V_{GS} is 0

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Plotting the Transconductance Curve

Using I_{DSS} and V_P (or $V_{GS(off)}$) values found in a specification sheet, the Family of Curves can be plotted by making a table of data using the following 3 steps:

Step 1:

Solve $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ for $V_{GS} = 0V$

Step 2

Solve $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ for $V_{GS} = V_P$ (aka $V_{GS(off)}$)

Step 3:

Solve $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ for $0V \geq V_{GS} \geq V_P$ in 1V increments for V_{GS}

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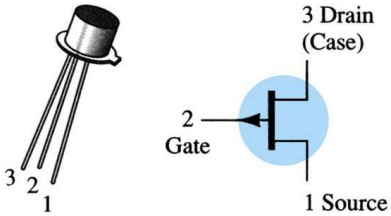
Case Construction and Terminal Identification

2N2844

CASE 22-03, STYLE 12
TO-18 (TO-206AA)



JFETs
GENERAL PURPOSE
P-CHANNEL

This information is found on the specification sheet

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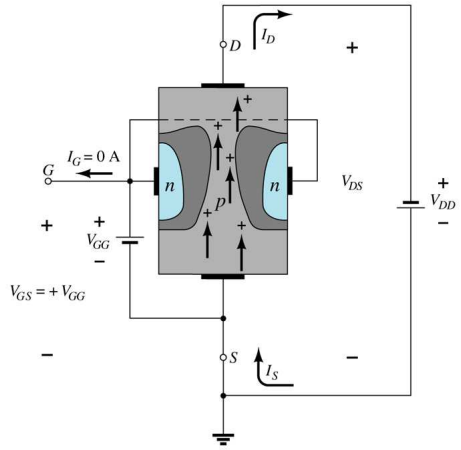
p-Channel JFET's



p-Channel JFET operates in a similar manner as the n-channel JFET except the voltage polarities and current directions are reversed

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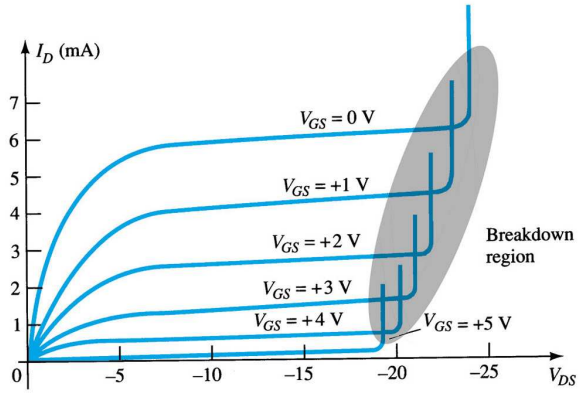
P-Channel JFET Characteristics



As V_{GS} increases more positively
- the depletion zone increases
- I_D decreases ($I_D < I_{DSS}$)
- eventually $I_D = 0$A

Also note that at high levels of VDS the JFET reaches a breakdown situation. ID increases uncontrollably if $V_{DS} > V_{DSmax}$.

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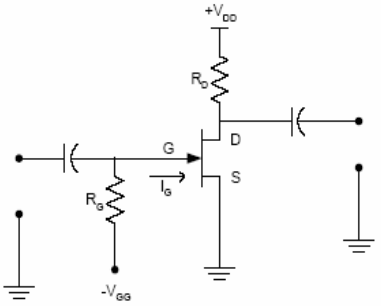
JFET Biasing Circuits Count...

Gate Bias: or Fixed Bias Ckt.



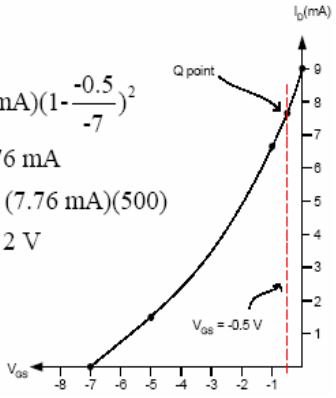
Since $I_G = 0$, $V_{GS} = V_{GG}$

$V_{DS} = V_{DD} - I_D R_D$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

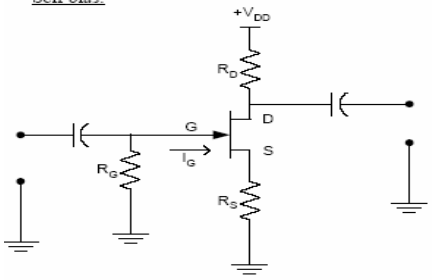
- Example: Determine the Q-point values for the gate biasing circuit if $V_{GG} = -0.5$ V, $V_{GS(off)} = -7$ V, $I_{DSS} = 9$ mA, $V_{DD} = 5$ V and $R_D = 500\Omega$.

$$I_D = (9\text{mA})\left(1-\frac{-0.5}{-7}\right)^2$$
$$= 7.76 \text{ mA}$$
$$V_{DS} = 5 - (7.76 \text{ mA})(500)$$
$$= 1.12 \text{ V}$$



JFET Self (or Source) Bias Circuit

Self bias:



Since $I_G = 0$, $V_G = 0$

$V_S = I_D R_S$

$V_{GS} = -I_D R_S$

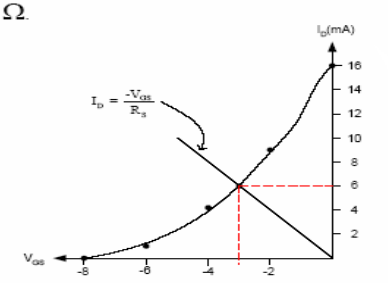
$$I_D = \frac{-V_{GS}}{R_S}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

and $$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\therefore I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = -\frac{V_{GS}}{R_S}$$

- Example: Determine the Q-point values for the self biasing circuit if $V_{GS(off)} = -8$ V, $I_{DSS} = 16$ mA, $V_{DD} = 10$ V, $R_D = 500\ \Omega$, $R_G = 1$ MΩ and $R_S = 500\ \Omega$.



$I_D = 6$ mA

$V_{DS} = 10 - (6\text{mA})(500+500)$

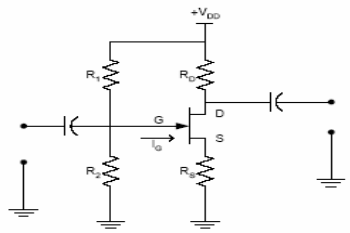
$= 4$ V

$$I_{DSS}\left[1 - 2\frac{V_{GS}}{V_P} + \left(\frac{V_{GS}}{V_P}\right)^2\right] + \frac{V_{GS}}{R_S} = 0$$

This quadratic equation can be solved for V_{GS} & I_{DS}

The Potential (Voltage) Divider Bias

Voltage-divider bias:



Since $I_G = 0$,

$$V_G = \frac{R_2}{R_1+R_2} V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$

The method used to plot the dc bias line for the voltage-divider bias is as follows:

1. Plot the transconductance curve for the specific JFET.
2. Calculate V_G.
3. Plot V_G on the positive x-axis.
4. Solve for I_D using $I_D = \frac{V_G}{R_S}$
5. Plot I_D found in (4) on the y-axis.
6. Extend the line to intersect the transconductance curve to obtain the Q-point values.

$$\therefore\ I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 - \frac{V_G - V_{GS}}{R_S} = 0$$

Solving this quadratic equation gives V_{GS} *and* I_{DS}

MOSFET's

MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful

There are 2 types of MOSFET's:

- Depletion mode MOSFET (D-MOSFET)
  - Operates in Depletion mode the same way as a JFET when $V_{GS} \leq 0$
  - Operates in Enhancement mode like E-MOSFET when $V_{GS} > 0$
- Enhancement Mode MOSFET (E-MOSFET)
  - Operates in Enhancement mode
  - $I_{DSS} = 0$ until $V_{GS} > V_T$ (threshold voltage)

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MOSFET Handling

MOSFETs are very static sensitive. Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can stablish an unwanted conduction.

Protection:

- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETS
- Apply voltage limiting devices between the Gate and Source, such as back-to-back Zeners to limit any transient voltage

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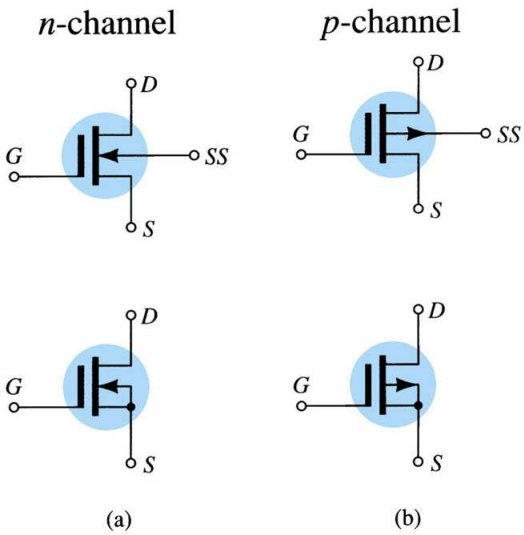
D-MOSFET Symbols



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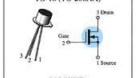
Specification Sheet

2N3797

CASE 22-03, STYLE 2
TO-18 (TO-206AA)



MOSFETs
LOW POWER AUDIO
N-CHANNEL – DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage 2N3797	V_{DS}	20	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage (V_{GS} = -7.0 V, I_D = 5.0 μA)	2N3797	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) (V_{GS} = -10 V, V_{DS} = 0) (V_{GS} = -10 V, V_{DS} = 0, T_A = 150°C)		I_{GSS}	– –	– –	1.0 200	pAdc
Gate Source Cutoff Voltage (I_D = 2.0 μA, V_{DS} = 10 V)	2N3797	$V_{GS(off)}$	–	-5.0	-7.0	Vdc
Drain-Gate Reverse Current (1) (V_{DG} = 10 V, I_S = 0)		$I_{D(GO)}$	–	–	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current (V_{DS} = 10 V, V_{GS} = +3.5 V)	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\lvert Y_{fs} \rvert$	1500	2500	3000	μmhos
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797		1500	–	–	
Output Admittance (I_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\lvert Y_{os} \rvert$	–	27	60	μmhos
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797	C_{iss}	–	6.0	8.0	pF
Reverse Transfer Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz, R_g = 3 megohms)		NF	–	3.8	–	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

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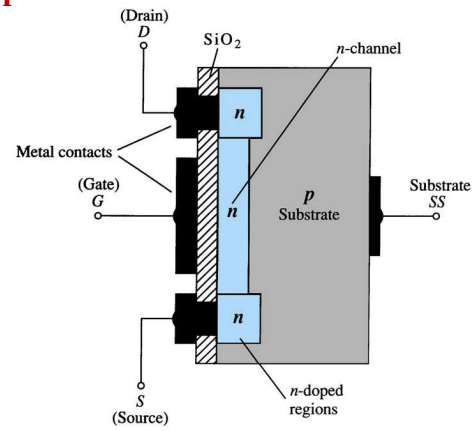
Depletion Mode MOSFET Construction



The Drain (D) and Source (S) leads connect to the to n-doped regions
These N-doped regions are connected via an n-channel
This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

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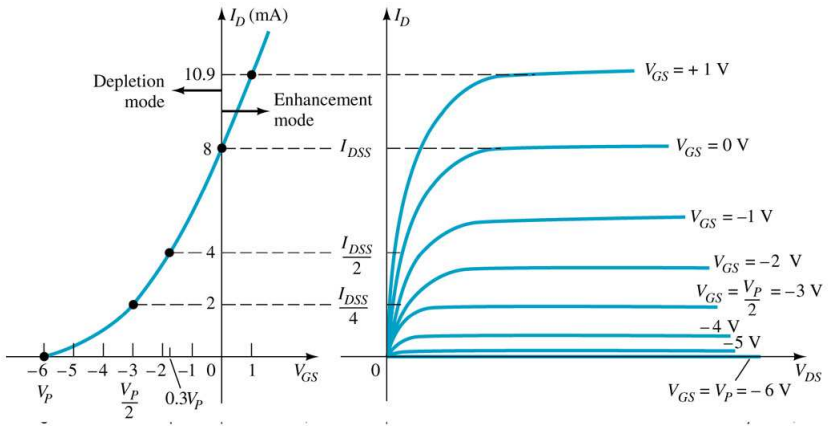
Basic Operation

A D-MOSFET may be biased to operate in two modes:
the **Depletion** mode or the **Enhancement** mode



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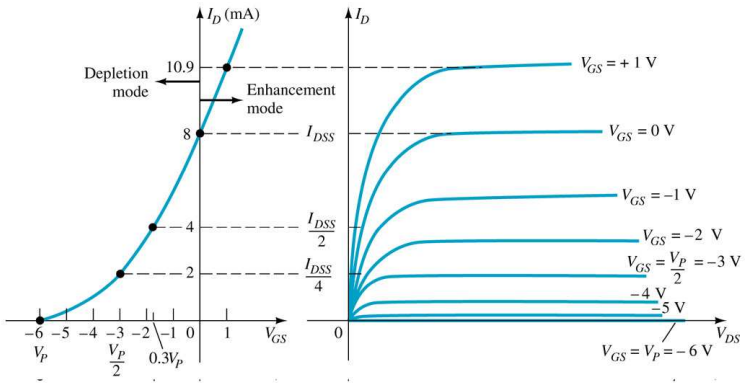
D-MOSFET Depletion Mode Operation



The transfer characteristics are similar to the JFET
In Depletion Mode operation:
When $V_{GS} = 0V$, $I_D = I_{DSS}$
When $V_{GS} < 0V$, $I_D < I_{DSS}$
When $V_{GS} > 0V$, $I_D > I_{DSS}$
The formula used to plot the Transfer Curve, is:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

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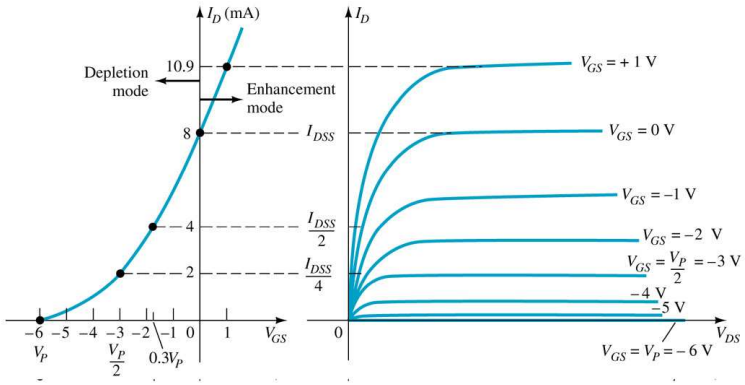
D-MOSFET Enhancement Mode Operation



Enhancement Mode operation
In this mode, the transistor operates with $V_{GS} > 0V$, and I_D increases above I_{DSS}
Shockley's equation, the formula used to plot the Transfer Curve, still applies but V_{GS} is positive:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

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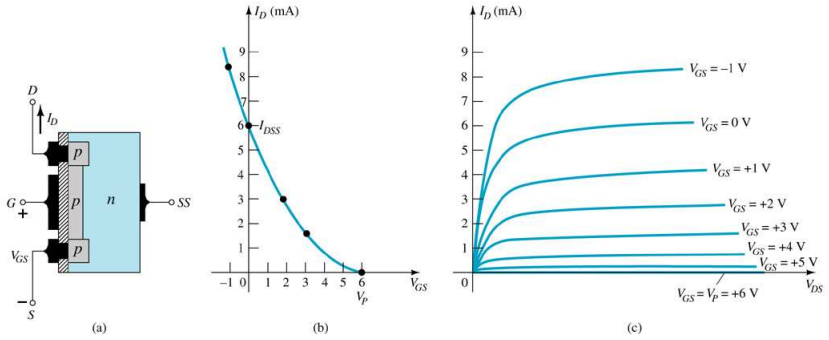
p-Channel Depletion Mode MOSFET



The p-channel Depletion mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed

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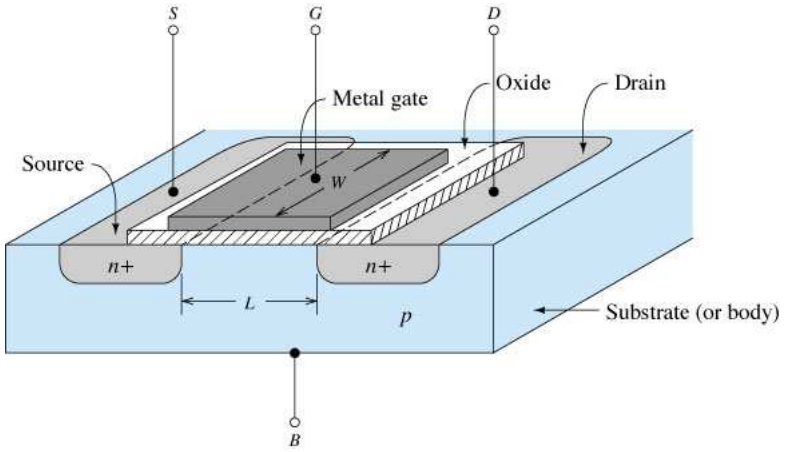
Enhancement Mode MOSFET's

n-Channel E-MOSFET showing channel length L and channel width W



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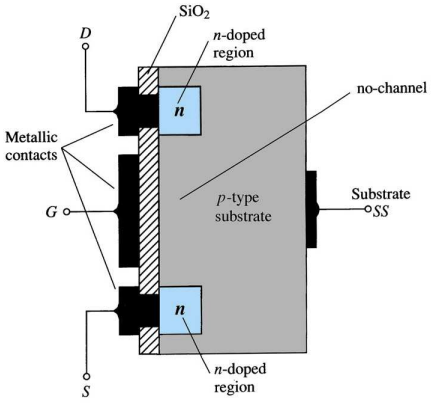
Enhancement Mode MOSFET Construction



The Drain (D) and Source (S) connect to the to n-doped regions
These n-doped regions are not connected via an n-channel without an external voltage
The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

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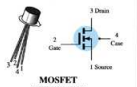
Specification Sheet

2N4351
CASE 20-03, STYLE 2
TO-72 (TO-206AF)



MOSFET SWITCHING
N-CHANNEL – ENHANCEMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_j	175	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0) T_A = 25°C T_A = 150°C	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current (V_{GS} = ± 15 Vdc, V_{DS} = 0)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage (I_D = 2.0 mA, V_{GS} = 10V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2.0 mA, f = 1.0 kHz)	$\lvert y_{fs} \rvert$	1000	–	μmho
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5)	t_{d1}	–	45	ns
Rise Time (Fig. 6)	t_r	–	65	ns
Turn-Off Delay (Fig. 7)	t_{d2}	–	60	ns
Fall Time (Fig. 8)	t_f	–	100	ns

(I_D = 2.0 mAdc, V_{DS} = 10 Vdc, (V_{GS} = 10 Vdc) (See Figure 9; Times Circuit Determined))

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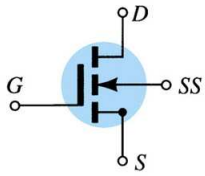
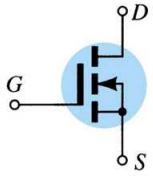
E-MOSFET Symbols

n-channel





(a)

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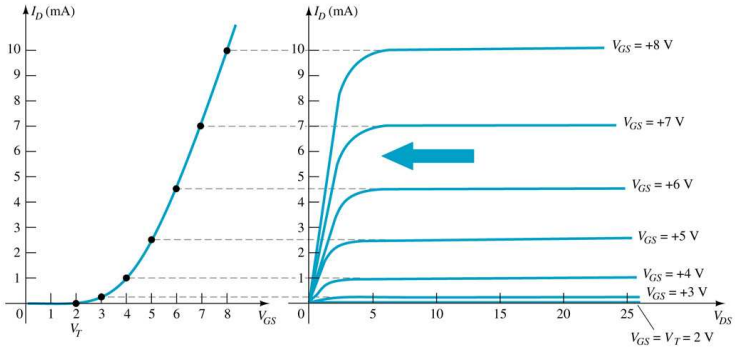
Basic Operation

The Enhancement mode MOSFET only operates in the enhancement mode.



V_{GS} is always positive
$I_{DSS} = 0$ when $V_{GS} < V_T$
As V_{GS} increases above V_T, I_D increases
If V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})
The saturation level, V_{DSsat} is reached.

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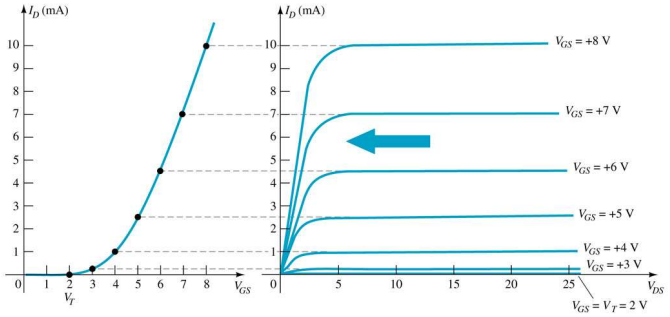
Transfer Curve



To determine I_D given V_{GS}: $\mathbf{I_D = k\,(V_{GS} - V_T)^2}$ $\qquad \mathbf{k = \dfrac{I_{D(on)}}{(V_{GS(ON)} - V_T)^2}}$

where V_T = threshold voltage or voltage at which the MOSFET turns on.
k = constant found in the specification sheet
The PSpice determination of k is based on the geometry of the device:

$$\mathbf{k = \left(\frac{W}{L}\right)\left(\frac{KP}{2}\right)} \quad \textbf{where } \mathbf{KP = \mu_N C_{OX}}$$

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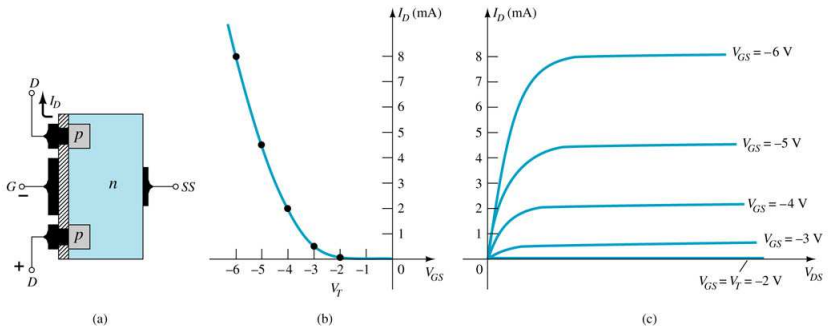
p-Channel Enhancement Mode MOSFETs

The p-channel Enhancement mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.



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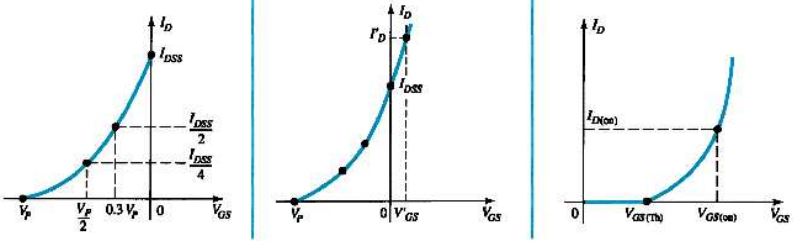
Summary Table

JFET	D-MOSFET	E-MOSFET
$I_G = 0$ A, $I_D = I_S$	$I_G = 0$ A, $I_D = I_S$	$I_G = 0$ A, $I_D = I_S$
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$I_D = k(V_{GS} - V_{GS(Th)})^2$, $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$



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